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Amendments to the Claims

1. (previously presented): A lateral FET structure comprising:

- a body of semiconductor material having a first conductivity type and a first major surface;
- a first well region of a second conductivity type formed in the body of semiconductor material;
- a second well region of the second conductivity type formed in the body of semiconductor material;
- a first drain contact region of the second conductivity type formed in a portion of the first well region;
- a second drain contact region of the second conductivity type formed in a portion of the second well region;
- a first doped region of the first conductivity type formed in another portion of the body of semiconductor material adjacent to the first well region;
- a first source region of the second conductivity type formed in the first doped region;
- a second doped region of the first conductivity type formed in a portion of the first well region adjacent to the first drain contact region;
- a gate structure formed over the first major surface;
- a first conductive layer coupled to the first source region to form a source contact;
- a second conductive layer formed over the body of semiconductor material and coupled to the first and second drain contact regions; and
- an interlayer dielectric layer separating at least a portion the first and second conductive layers.

2. (original): The structure of claim 1 wherein the first doped region surrounds the first well region.

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3. (previously presented): The structure of claim 1 further comprising a second source region formed in the body of semiconductor material, wherein the first conductive layer is coupled to the second source region.

4. (previously amended): The structure of claim 1 further comprising a third doped region of the first conductivity type surrounding the second well region, and wherein the first and third doped regions are absent a fingertip region.

5. (original): The structure of claim 1 wherein the first drain region comprises an elongated stripe shape.

6. (original): The structure of claim 5 wherein the first source region comprises an elongated stripe shape substantially parallel to the first drain region.

7. (original): The structure of claim 1 wherein the first and second well regions are spaced apart.

8. (original): The structure of claim 1 wherein the first well region includes a pair of opposing rounded tips.

Claim 9 (cancelled).

10. (original): The structure of claim 1 wherein the first conductive layer and second conductive layer do not overlap.

11. (original): The structure of claim 1 wherein a portion of the second conductive layer is over a portion of the first well region and separated from the first well region by a dielectric layer.

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Claims 12-16 (cancelled).

17. (previously presented): A method for forming a lateral FET device comprising the steps of:

providing a body of semiconductor material having a first conductivity type;

forming a plurality of drain regions in the body of semiconductor material;

forming a plurality of source regions in the body of semiconductor material;

forming a first conductivity type doped region in at least one of the plurality of well regions;

forming a first conductive layer on the body of semiconductor material and coupled to the plurality of drain regions; and

forming a second conductive layer on the body of semiconductor material and coupled to the plurality of source regions, wherein at least a portion of the second conductive layer is separated from a portion of the first conductive layer by a dielectric layer.

18. (original): The method of claim 17 wherein the step of forming the plurality of drain regions comprises the steps of:

forming a plurality of well regions in the body of semiconductor material, and

forming a drain contact region in at least one of the plurality of well regions.

Claim 19 (cancelled).

20. (original): The method of claim 17 wherein the step of forming the second conductive layer includes forming a second

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conductive layer wherein portions of the second conductive layer terminate in proximity to the first conductive layer.

21. (currently amended): A lateral FET device comprising:
a semiconductor substrate having a first conductivity type;
a plurality of drain regions of a second conductivity type formed in the semiconductor substrate, ~~body of semiconductor material~~, wherein each drain region comprises a well region and a drain contact region;

a plurality of source regions of the second conductivity type formed in the semiconductor substrate; ~~body of semiconductor material~~;

a first conductive layer formed over the semiconductor substrate, ~~body of semiconductor material~~, wherein the first conductive layer couples at least two source regions together;

a second conductive layer formed over the semiconductor substrate, ~~body of semiconductor material~~, wherein the second conductive layer couples at least two drain contact regions together; and

a dielectric layer formed over the semiconductor substrate, ~~body of semiconductor material~~, wherein the dielectric layer vertically separates the first and second conductive layers.

22. (currently amended): The device of claim 21 further comprising a ~~plurality of doped regions~~ doped region of the first conductivity type, wherein ~~one of the plurality of source regions is within one of the plurality of doped regions~~, are formed in the doped region, and wherein ~~one of the plurality of doped regions~~ the doped region surrounds one well region.

23. (previously presented): The device of claim 21 wherein one well region includes a pair of opposing rounded tips.

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24. (previously presented): The device of claim 21 further comprising a doped region of the first conductivity type surrounding at least one well region, wherein the doped region is absent a fingertip region.

25. (currently amended): The device of claim 21 wherein at least one drain contact region comprise an elongated stripe shape having rounded tips at opposing ends.

26. (currently amended): The device of claim 21 wherein [[a]] one well region has an edge at a surface of the semiconductor substrate, and wherein a portion of the second conductive layer is formed to extend over the edge. ~~a portion of one well region and separated from the one well region by a dielectric layer.~~